B. AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A memory shared by a plurality of heterogeneous processors, comprising:

the shared memory;

wherein the shared memory is accessible by one or more first processors that are adapted to process a first instruction set;

wherein the shared memory is accessible by one or more second processors that are adapted to process a second instruction set;

wherein the shared memory is partitioned into a non-private memory area that is accessible by one or more of the first processors and one or more of the second processors;

wherein one of the second processors is adapted to access a private memory area that is not accessible by any of the first processors; and

a memory map corresponding to the shared memory, wherein the memory map includes cross-references between virtual addresses and real addresses, the memory map and the cross-references shared between the first processors and the second processors.

2. (Canceled)

3. (Previously Presented) The shared memory as described in claim 1 further comprising:

an operating system that operates on one of the first processors, the first processor controlling the memory map.

4. (Original) The shared memory as described in claim 1 wherein each second processor further comprises:

a synergistic processing unit;

a local storage; and

a memory management unit, the memory management unit including a direct memory access controller.

5. (Original) The shared memory as described in claim 4 wherein at least one of the second processors use the direct memory access controller to access the shared memory.

6. (Canceled)

7. (Canceled)

8. (Previously Presented) The shared memory as described in claim 1 wherein the memory map includes a plurality of regions, wherein at least one of the regions is selected from the group consisting of an external system memory region, a local storage aliases region, a TLB region, an MFC region, an operating system region, and an I/O devices region.

9. (Canceled)

10. (Canceled)

11. (Canceled)

12. (Canceled)

13. (Canceled)

14. (Canceled)

15. (Canceled)

16. (Canceled)

17. (Canceled)

18. (Currently Amended) A computer program product stored on a computer operable media, the computer operable media containing instructions for execution by a computer, which, when executed by the computer, cause the computer to implement a method for sharing a memory between a plurality of heterogeneous processors, the method comprising:

allocating a first memory partition on the shared memory that corresponds to the memory request, the first memory partition accessible by one or more first processors that are adapted to process a first instruction set;

assigning a second memory partition on the shared memory to one or more second processors that are adapted to process a second instruction set, wherein the first processors and the second processors are heterogeneous;

wherein the shared memory is partitioned into a non-private memory area that is accessible by one or more of the first processors and one or more of the second processors;

wherein one of the second processors is adapted to access a private memory area that is not accessible by any of the first processors;

managing the first memory partition and the second memory partition using a common memory map that includes a plurality of regions, wherein at least one of the regions

is selected from the group consisting of an external system memory region, a local storage aliases region, a TLB region, an MFC region, an operating system region, and an I/O devices region; and

wherein the TLB region includes cross-references between virtual addresses and real addresses, the common memory map and the cross-references shared between the first processors and the second processors.

19. (Canceled)

20. (Previously Presented) The computer program product as described in claim 18 wherein one of the first processors includes an operating system whereby the first processor controls the common memory map.

21. (Canceled)

22. (Original) The computer program product as described in claim 18 wherein at least one of the first processors is a Power PC and wherein at least one of the second processors is included in a synergistic processing unit.

23. (Original) The computer program product as described in claim 22 wherein the shared memory corresponds to the synergistic processing unit.

24. (Original) The computer program product as described in claim 18 wherein at least one of the second processors uses a direct memory access controller for accessing the shared memory.

25. (Currently Amended) A memory shared by a plurality of heterogeneous processors, comprising:

the memory, wherein the memory includes one or more non-private storage areas, the non-private storage areas included in one or more second processors that are adapted to process a second instruction set and access the memory;

wherein the ~~shared memory is~~ non-private storage areas are accessible by one or more first processors that are adapted to process a first instruction set and access the memory;

wherein one of the second processors is adapted to access a private memory area that is not accessible by any of the first processors;

and

a memory map corresponding to the shared memory, wherein the memory map includes cross-references between virtual addresses and real addresses, the memory map and the cross-references shared between the first processors and the second processors.

26. (Original) The shared memory as described in claim 25 wherein each second processor further comprises:

synergistic processing logic which uses private storage, the private storage not included in the shared memory; and

memory management logic for directly accessing the shared memory.

27. (Original) The shared memory as described in claim 25 further comprising:

memory mapping logic that corresponds to the shared memory, wherein the memory mapping logic is shared between the first processors and the second processors.

28. (Original) The shared memory as described in claim 27 further comprising:

an operating system that operates on one of the first processors, the first processor controlling the memory mapping logic.

29. (Original) The shared memory as described in claim 25 wherein one of the first processors configures each of the non-private storage areas.

30. (Previously Presented) The shared memory as described in claim 1 further comprising:

wherein the shared memory, the first processors, and the second processors are included on one silicon substrate and are connected using an on chip coherent multi-processor bus.